Ch. 4 Von Neumann

4.1 Name the five components of the von Neumann model. For each component, state its purpose.

The five components of the von Neumann model are:

1. Memory, which is the storage of information

2. Processing Unit, which processes information

3. Input, which is tools used to provide information to the computer

4. Output, which provides information from the computer

5. Control Unit, which is what makes all the parts work together

4.2 Briefly describe the interface between the memory and the processing unit. That is, describe the method by which the memory and the processing unit communicate.

The communication is done mainly by the Memory Address Register and the Memory Data Register. To read, the address of the location is put in to the MAR, enabled to be read, and the value is put in MDR. To write, the location is put in to the MAR, is put in the MDR, and the value is written to the location.

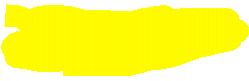
4.6 What are the two components of an instruction? What information do these two components contain?

The two components of an instruction are the opcode and the operands. The opcode is what the instruction does, and the operands is the subjects of the operations

4.7 Suppose a 32-bit instruction takes the following format:

OPCODE SR DR IMM

If there are 60 opcodes and 32 registers, what is the range of values that can be represented by the immediate (IMM)? Assume IMM is a 2's complement value.



4.9 The FETCH phase of the instruction cycle does two important things. One is that it loads the instruction to be processed next into the IR. What is the other important thing?

It increments the PC to point to the next instruction

4.11 State the phases of the instruction cycle and briefly describe what operations occur in each phase.

There are six phases:

1. Fetch: You first load the MAR with the contents of the program counter and simultaneously increments the PC register. Also, it fetches the actual memory from the address given from the MAR and is placed into the MDR. Finally, it loads the IR with the contents of the MDR.

2. Decode: Examine the instruction so see what the processor is being asked to do and what opcode needs to process.

3. Evaluate Address: Computes the address of the memory location.

4. Fetch Operands: Obtains source operands required to process instruction.

5. Execute: Actual execution of Instruction.

6. Store Address: Stores the result of execution